

OHMEGA-PLY® INTEGRAL PLANAR RESISTORS: THE LOWER COST ALTERNATIVE

By
Daniel Brandler
Ohmega Technologies, Inc.

Printed circuit board designers are being forced to interconnect electronic devices of increasing I/O densities in smaller and smaller circuit board surface areas. This has resulted in the growing use of new circuit board technologies such as HDI, blind and buried vias, microvias and integral passive devices.

There are numerous applications where package densification, electrical performance and/or reliability are the main objectives of the circuit board designer. In these applications, circuit board technologies are selected for use based on design, rather than economic, reasons. In many circuit board designs, however, cost is of primary importance and is the main determinate in which technologies are used in high-density applications.

The perceived risks and higher costs associated with using integral passive devices are major concerns of the design community; however, Ohmega-Ply® has been in volume production use in a variety of applications for over 25 years with a track record of superior performance and high reliability. In addition, the shift to newer circuit board technologies of greater interconnect densities makes the use of Ohmega-Ply® an extremely cost effective alternative to discrete components.

Ohmega-Ply® is an Integral Planar (IP) resistor technology in which thin-film resistive elements are formed by using standard subtractive printed circuit board print-and-etch processing. These resistive elements are typically used as buried resistors in multilayer printed wiring boards or other high density interconnecting substrates. Ohmega-Ply® IP designs are created with CAD/CAM layout tools. Resistor elements are shaped by simple design rules. The resistors are placed on existing layers depending on their function (i.e. parallel terminations on power planes; series termination on signal/logic planes). No new circuit layers are required.

The focus of this paper will be to review how Ohmega-Ply® can be cost effective in high-density circuit designs by reducing the overall substrate cost as well as by eliminating both the procurement and assembly of discrete surface mount resistors.

Since conventional subtractive print and etch technologies are used to create the resistors, the area cost of the Ohmega-Ply® material remains fixed, as does the processing costs, regardless of the number of resistors created. Therefore, the unit cost of an Ohmega-Ply® resistor declines in proportion to the increase in the number of resistive elements required. Simple cost models have been employed to compare the unit cost of using Ohmega-Ply® to the number of resistive elements in a given area. Table 1 is one such cost model.

This cost model compares the fixed Ohmega-Ply[®] area cost to SMT chip resistor cost at various component densities. The cost of a chip resistor is an aggregate of its procurement and assembly costs and will vary by application, volume and OEM or contract assembler. In Table 1 a range of \$0.01 to \$0.05 per chip resistor is used although the actual cost may be either lower or higher than this range. The conversion cost of Ohmega-Ply[®] (material and processing costs) will also vary by application, volume and board shop. The price charged by a board shop using Ohmega-Ply[®] normally ranges from 1.5 to 2.0 times the material cost. Based on this formula, the added cost (per square inch of board area) to a circuit board using a layer of Ohmega-Ply[®] is as follows:

	<u>Volume:</u>	<u>Prototype</u>	<u>Low</u>	<u>Medium</u>	<u>High</u>
Ohmega-Ply [®] Material		\$0.25	\$0.20	\$0.15	\$0.11
Board conversion cost		\$0.37-\$0.50	\$0.30-\$0.40	\$0.22-\$0.30	\$0.16-\$0.22

The volume costs above are based on a low volume annual requirement of approximately 1,000 square feet, a medium volume annual requirement of approximately 30,000 square feet and a high volume annual requirement of approximately 250,000 square feet.

Based on the above costs, breakeven occurs between four and ten resistors per square inch of board area (or about 1 resistor per cm²). However, this cost model does not take into consideration comparative substrate costs. The breakeven point merely shows the component density at which it becomes cost effective to utilize Ohmega-Ply[®] as a replacement for SMT chip resistors.

This simple analysis does not include other potential cost savings in using Ohmega-Ply[®] such as reduced layer counts, reduced form factors and conversion of double sided to single sided SMT. Improved wireability due to the elimination of vias may allow a design to eliminate one or more layers of a multilayer circuit board. These other potential cost savings would reduce the resistor density required for breakeven.

A more realistic cost model must take into consideration substrate and assembly metrics, component density, I/O density and wiring density. In fact, these are the primary determinates of when it is cost effective to use the Ohmega-Ply[®] IP technology. The cost impact of using SMT chip resistors becomes significant as increasing circuit densities force a shift to more expensive interconnect technologies. These technology shifts are (in order of increasing complexity):

- Single-sided SMT changes to double-sided SMT
- Standard multilayer PCBs become sequentially built PCBs with buried vias
- Standard multilayer PCBs become HDI substrates with or without microvias

The switch to Ohmega-Ply[®] occurs when higher cost PCBs or HDI substrates must be used to interconnect SMT resistors. Embedding resistors into existing layers of a circuit board and using conventional PCB processing reduces the cost of the substrate by allowing for more conventional PCB technologies to be used.

The cost advantages of Ohmega-Ply[®] are:

- Reduced substrate area costs resulting from smaller form factors
- Reduced substrate conversion costs (less need for added layers, build-up and/or HDI technologies)

Higher levels of interconnection within the circuit board are necessary when active components densities and lead counts increase. This higher interconnection can be achieved through the use of finer lines and spaces, blind and buried vias, greater layer counts and HDI substrates. These technologies include microvias and/or build-up layer technologies that add significant cost to the substrate. In addition, the higher component densities add cost to the assembled board.

By using Ohmega-Ply[®] the total area required for component placement and interconnection decreases. For high-speed digital electronics with passive to active component ratios greater than 15 to 1, the area cost reduction can exceed 30% of the total board area. Furthermore, if increased component and I/O densities force a change in board construction to incorporate advanced technologies like blind and buried vias or microvias, then using Ohmega-Ply[®] will allow for simpler—and less costly—circuit boards.

The additional cost to the final circuit board using Ohmega-Ply[®] was shown to be approximately \$0.16 to \$0.40 per square inch of board area depending on volume. When the area cost increase of an alternative design using advanced circuit technology without Ohmega-Ply[®] exceeds this amount then the use of Ohmega-Ply[®] is compelling.

However, the OEM and/or designer may not recognize the potential cost savings of Ohmega-Ply[®] until after an alternative and more expensive technology is adopted. What is needed then for design cost optimization is an advanced technology cost model that predicts HDI substrate and passive SMT costs based on density metrics.

The advanced technology cost model (Table 2) shows that density metrics such as component density, I/O density and wiring density (interconnectivity) are the primary determinates of the use of integral passive components for cost optimization. This model shows that Ohmega-Ply[®] use is indicated at complexity levels of 100 to 200 I/Os per square inch or interconnect densities of 100 to 160 inches per square inch. Continued use of discrete SMT resistors beyond this range drives up costs as increasing densities force the shift to more expensive interconnect technologies.

These density metrics are a measure of substrate and assembly complexity and cost and are based on comparative PCB designs. The wiring density numbers are calculated by standard interconnectivity equations that relate component pitch and density (I/O's per part and parts per square inch) to inches per square inch of wiring.

Following is a comparison of some of these technologies (per square inch of board area). The comparison is based on an application requiring 10 resistors per square inch of board area:

<u>Substrate Type</u>	<u>Cost Adder Substrate</u>	<u>Total Cost bare board</u>	<u>SMT Cost (resistors)</u>	<u>Total Cost, Bare board + resistors</u>
Standard 6-lyr w/SMT	----	\$0.12	\$0.20	\$0.32
Standard 6-lyr w/Ohmega	\$0.20	\$0.32	----	\$0.32
Microvia 4-lyr w/SMT	\$0.46	\$0.58	\$0.20	\$0.66
Sequential Build 6-lyr (buried vias w/SMT)	\$0.49	\$0.61	\$0.20	\$0.81

Source: NEMI Draft Technical roadmap 2000

In most applications the PCB designer will use the lowest cost technology available that meets the product specifications, performance and reliability requirements. Although added material cost of using Ohmega-Ply[®] as a replacement for SMT chip resistors is a factor, the more significant cost adder to a circuit design is the shift to a more advanced board technology than is necessary due to a lack of board area real estate or the use of array packaging and the need to terminate leads within the array. As a result, resistor densities far lower than those indicated in the Table 1 cost model can justify the use of Ohmega-Ply[®] for economic reasons.

In addition to the other benefits of Ohmega-Ply[®], it is the opportunity for substrate cost reduction plus the coat advantages arising from the elimination of SMT chip resistors that will drive the use of Ohmega-Ply[®]. For a given design, the maximum component density, the average I/O density and the required interconnectivity (inches/square inch of wiring) are the primary determinates of the use of Ohmega-Ply[®] IP resistors for cost optimization. As technology forces the designer to more advanced circuit board technologies, Ohmega-Ply[®] becomes the lower cost alternative.

Typical Board Cost Adder Per Layer of Various (Discount) Levels

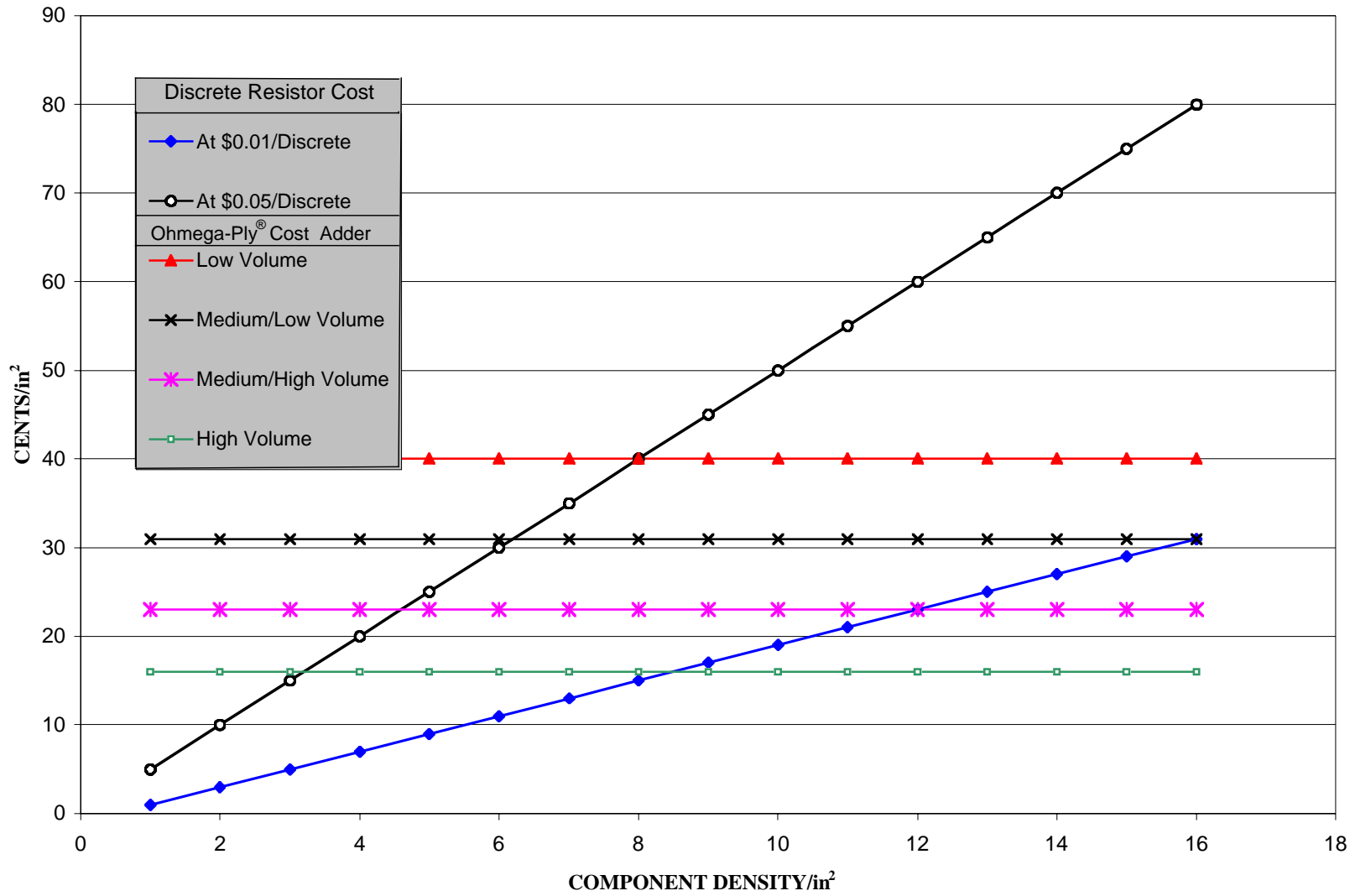
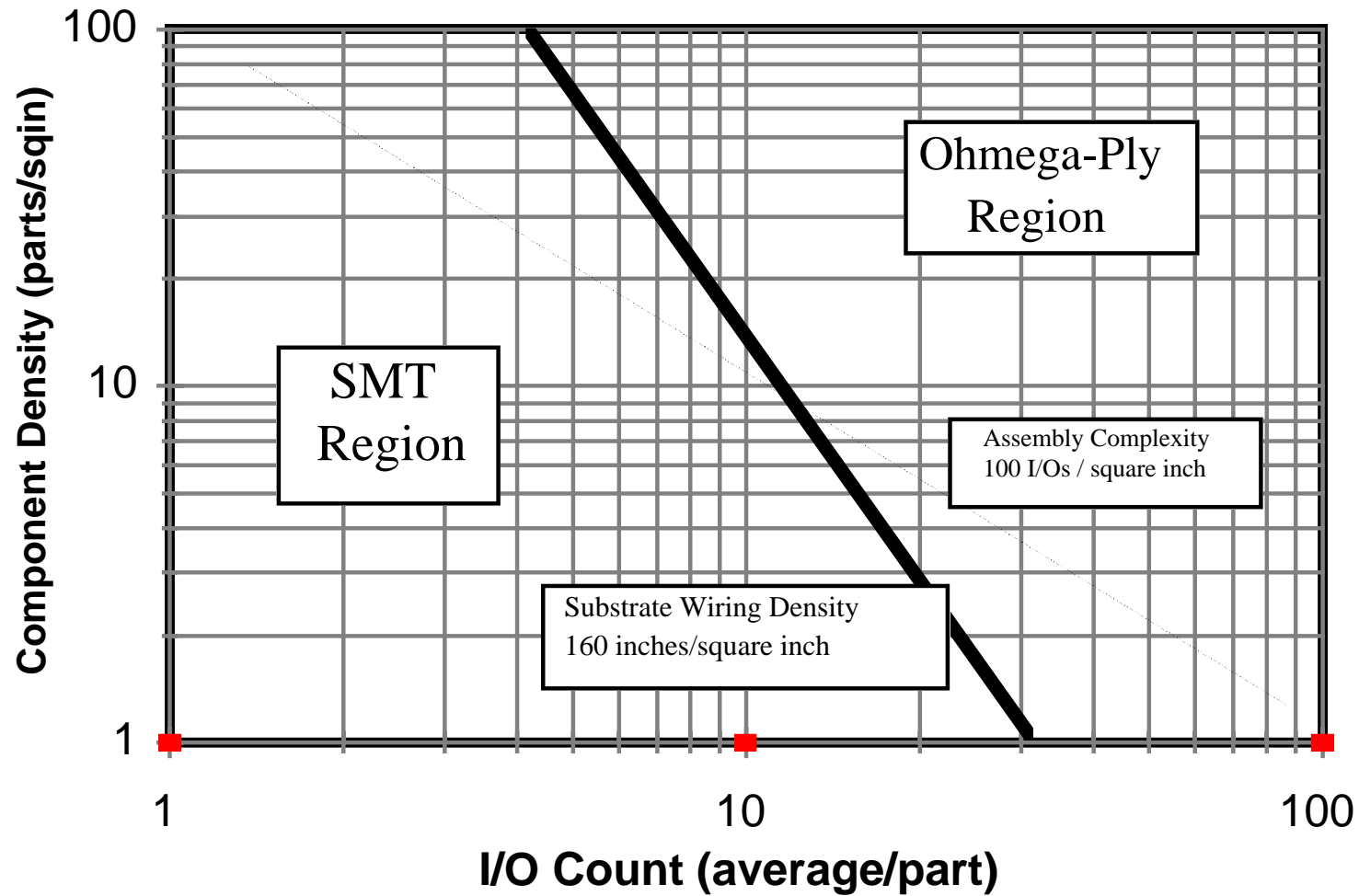


TABLE 1

Advanced Technology Chart SMT versus Ohmega-Ply



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Table 2